

# The Fundamentals of Ds3: Part 1

A working knowledge of DS3 multiplexing aids in an overall understanding of T-carrier issues.

Gregory R. Werth

*Part I of this article covers the M13 format and the multiplexing process involved in forming a DS3 signal from multiple DS1s. Part II, in the September issue, will cover the C-bit parity format and the advantages it provides over the M13 format.*

OVERVIEW

To meet the growing demands for voice and data communications, America's largest corporations are exploring the high-speed worlds of optical fiber and DS3 circuits. As end users continue to demand

more throughput, the move to DS3 circuits is often the best solution for DS1-based private networks. Today's DS3 tariff rates are designed to attract customers, even if these customers can't immediately take advantage of the extra bandwidth. Depending upon location and distance, a DS3 circuit will cost about the same amount as four to ten DS1 circuits. Once the jump to DS3 bandwidth is made, users have a cost-effective means of implementing a host of new communication technologies, including videoconferencing, workstation-based graphics, distributed data processing, and more advanced facsimile transmission.

Due to the increasing presence of DS3 circuits, understanding the DS3 channel is imperative. This two-

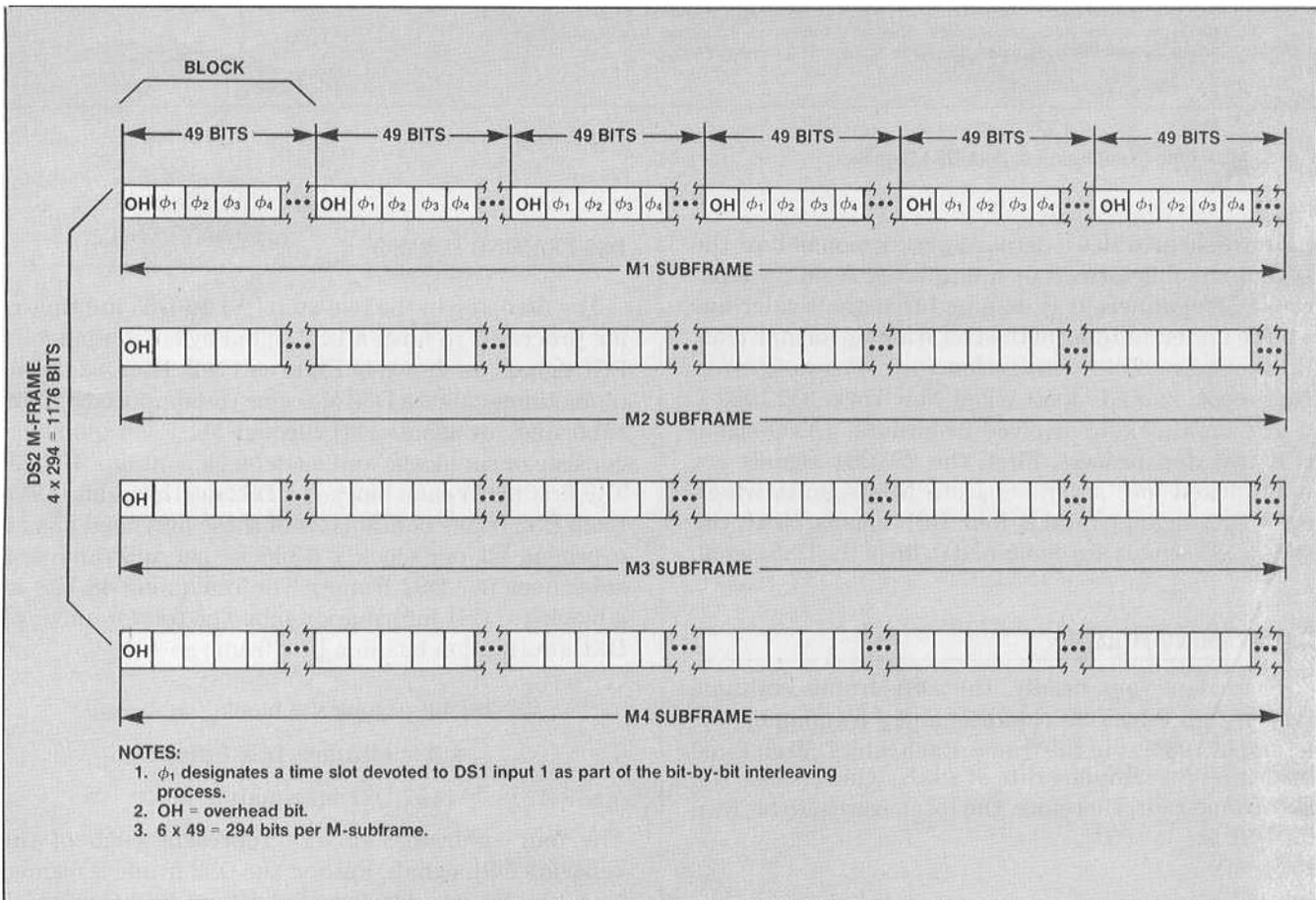


Fig. 1. DS2 Framing Format.

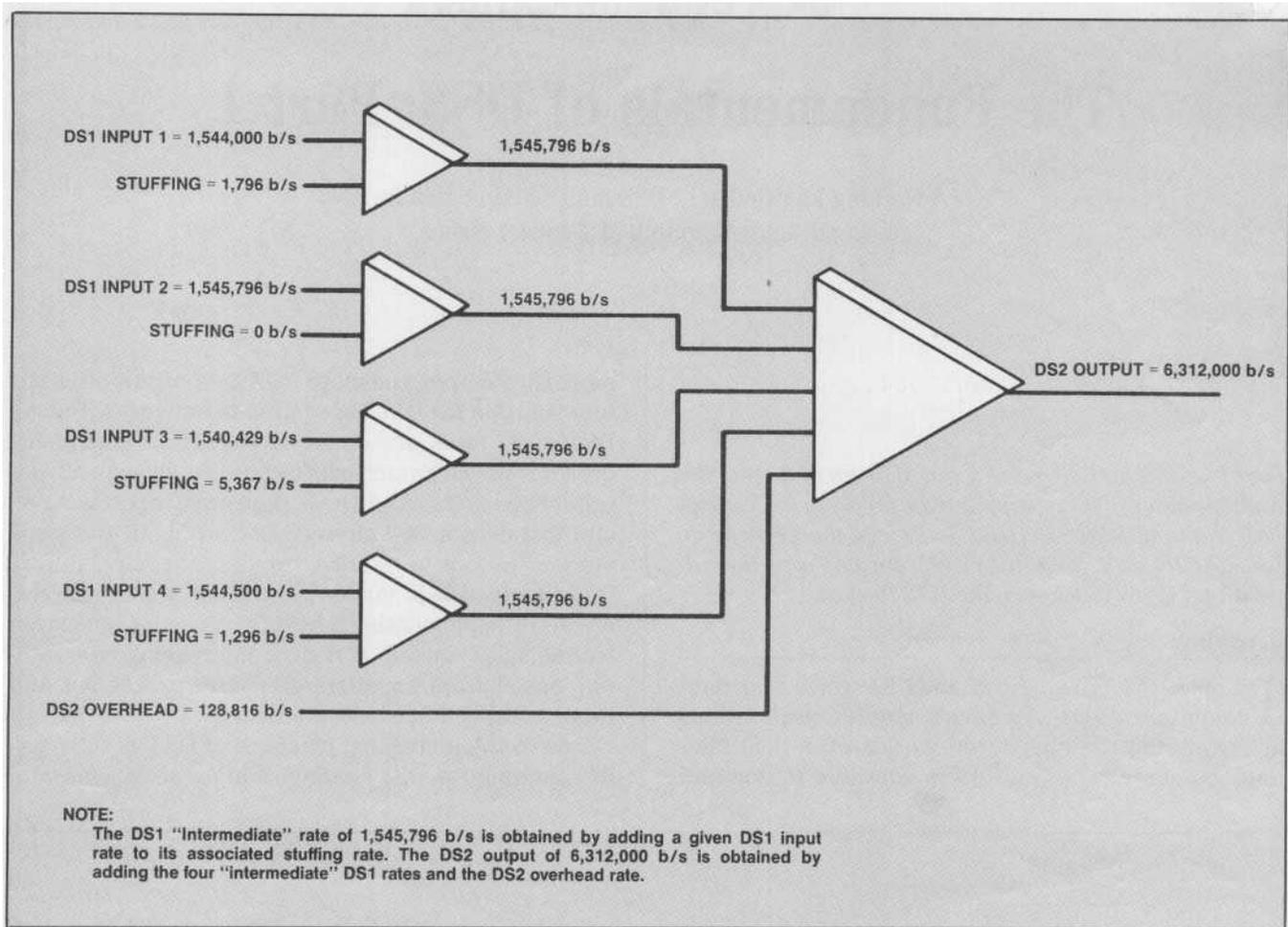


Fig. 2. M13-Type Multiplexing of Four DS1 Signals.

part article provides a detailed description of how the DS3 channel is formed or multiplexed from 28 separate DS1 channels. It is assumed that the reader has a basic understanding of the DS1 framing format. (Ref. R. Freeman, *Telecommunications Transmission Handbook*, 2nd ed., John Wiley, New York, NY, 1982.)

The multiplexing involved in forming a DS3 signal is a two-step process. First, the 28 DS1 signals are multiplexed into seven separate DS2 signals, where each DS2 signal contains four DS1 signals. Next, the seven DS2 signals are combined to form the DS3 signal.

#### DS1 FRAMING FORMAT

To review very briefly, the DS1 frame contains twenty-four 8-bit DSO channels and a framing bit, for a total of 193 bits in the frame. Each 8-bit DSO channel operates at a sampling rate of 8 kHz, which is also the DS1 frame rate. Therefore, the total aggregate bit rate for DS1 is:

$$193 \text{ bits/frame} \times 8000 \text{ frames/sec} = 1.544 \text{ Mbps,}$$

which is the nominal bit rate for DS1.

#### DS2 FRAMING FORMAT

The first step in the two-step DS1-to-DS3 multiplexing process is to form a DS2 signal by combining four DS1 signals, as shown in Figures 1 & 2. The DS2 frame (sometimes called a DS2 M-frame) is composed of four subframes, designated M1 through M4. Each subframe consists of six blocks and each block contains 49 bits. The first bit in each block is a DS2 overhead bit (OH). Each DS2 frame contains 24 of these overhead bits (1 overhead bit per block x 6 blocks per subframe x 4 subframes per DS2 frame). The remaining 48 bits in a block are DS1 information bits. The total number of DS1 information bits in a DS2 frame is:

$$\begin{aligned} &48 \text{ DS1 bits/block} \times 6 \text{ blocks/subframe} \\ &\quad \times 4 \text{ subframes/DS2 frame} \\ &= 1152 \text{ DS1 information bits.} \end{aligned}$$

The four subframes do not represent each of the separate DS1 signals. Rather, the DS2 frame is formed by bit-by-bit interleaving of the four DS1 signals, as demonstrated in Figure 1. Note that each block in every subframe has the bit sequence labeled as OH,  $\phi_1$ ,

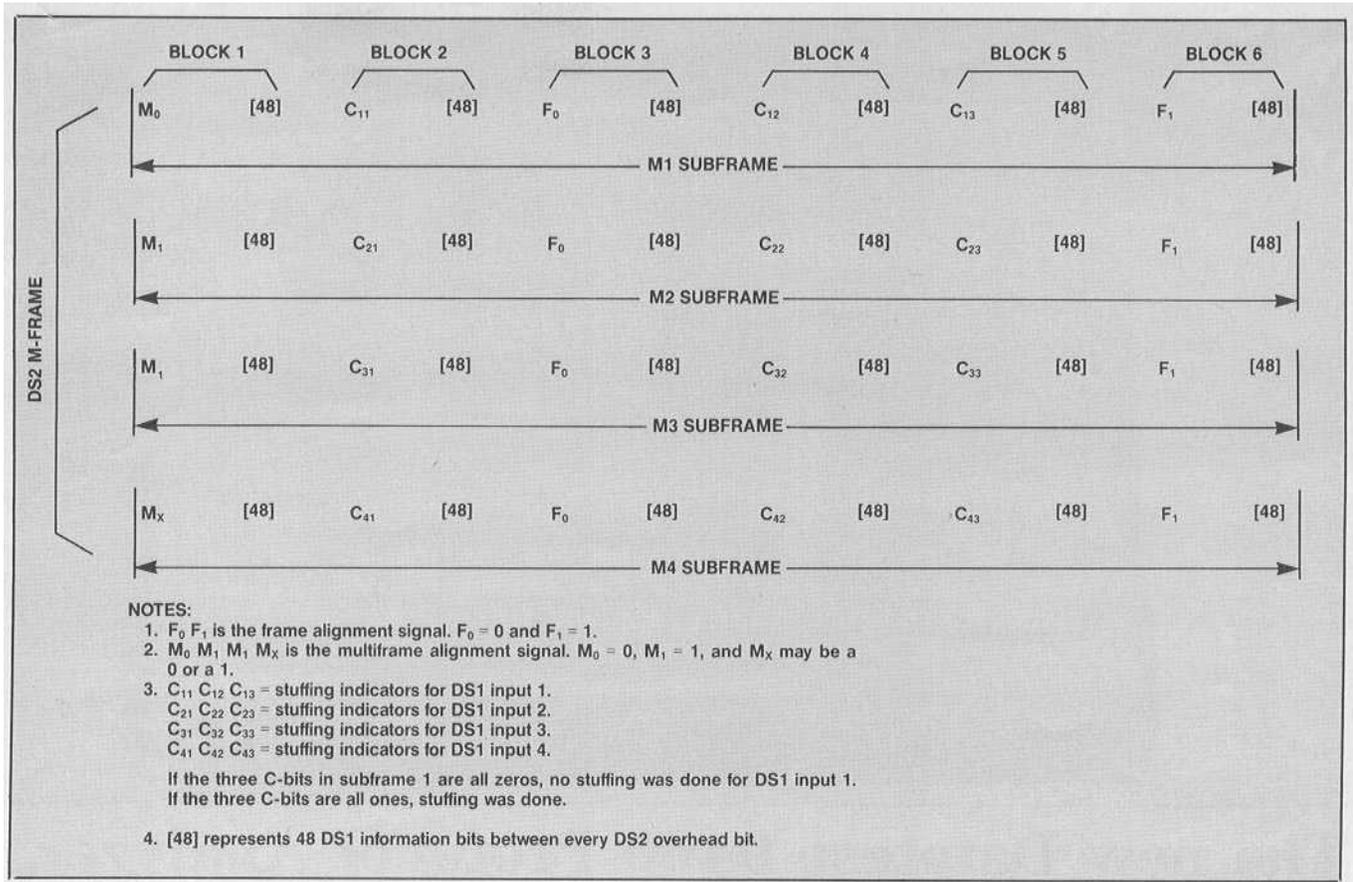


Fig. 3. DS2 Overhead Bits.

$\phi_2, \phi_3, \phi_4$ , etc. The OH leads off every block and is followed by the interleaved DS1 data bits where  $\phi_i$  designates the time slot devoted to DS1 input  $i$ . After every 48 DS1 information bits - 12 from each DS1 signal - a DS2 overhead bit is inserted. The total number of DS1 information bits transmitted in one second in a DS2 frame is:

$$\text{DS1 rate} \times 4 \text{ DS1 signals/DS2,}$$

which is:

$$1.544 \text{ Mbps} \times 4 \text{ DS1 signals/DS2} = 6.176 \text{ Mbps.}$$

The overall rate used for DS2 is 6.312 Mbps, which provides extra bandwidth for DS2 bit stuffing and DS2 overhead bits.

### DS2 Bit Stuffing

The four DS1 signals are asynchronous relative to each other, and therefore may be operating at different rates. A synchronization method used by multiplexers, called bit stuffing (or pulse stuffing), is used to adjust the different incoming rates. (Bit stuffing will be further explained in Part 11.)

### DS2 Overhead Bits

The DS2 overhead bits provide alignment and bit stuffing control. The overhead bits are located in the

first bit position of every block. Figure 3 shows the location of the various DS2 overhead bits designated F, M, and C.

### F-bits

The F-bits (framing bits) form the frame-alignment signal. There are eight F-bits per DS2 frame (two per subframe). The F-bits are located in the first bit position in blocks 3 and 6 of each subframe. The frame-alignment pattern, which is repeated every subframe, is "01."

The rate of framing-bit errors is a good in-service approximation of the logic bit error rate, because of the number and location of framing bits.

### M-bits

The M-bits (multiframe bits) form the multiframe-alignment signal. There are four M-bits per DS2 frame (one per subframe). The M-bits are located in the first bit position in each subframe. Transmission equipment uses the M-bit pattern, "011X" (where X can be a "0" or a "1"), to locate the four subframes.

### C-bits

The C-bits are used to control bit stuffing. There are three C-bits per subframe, designated  $C_j$  (see Figure 3), where  $i$  corresponds to the subframe number and  $j$  refers to the position number of the C-bit in a

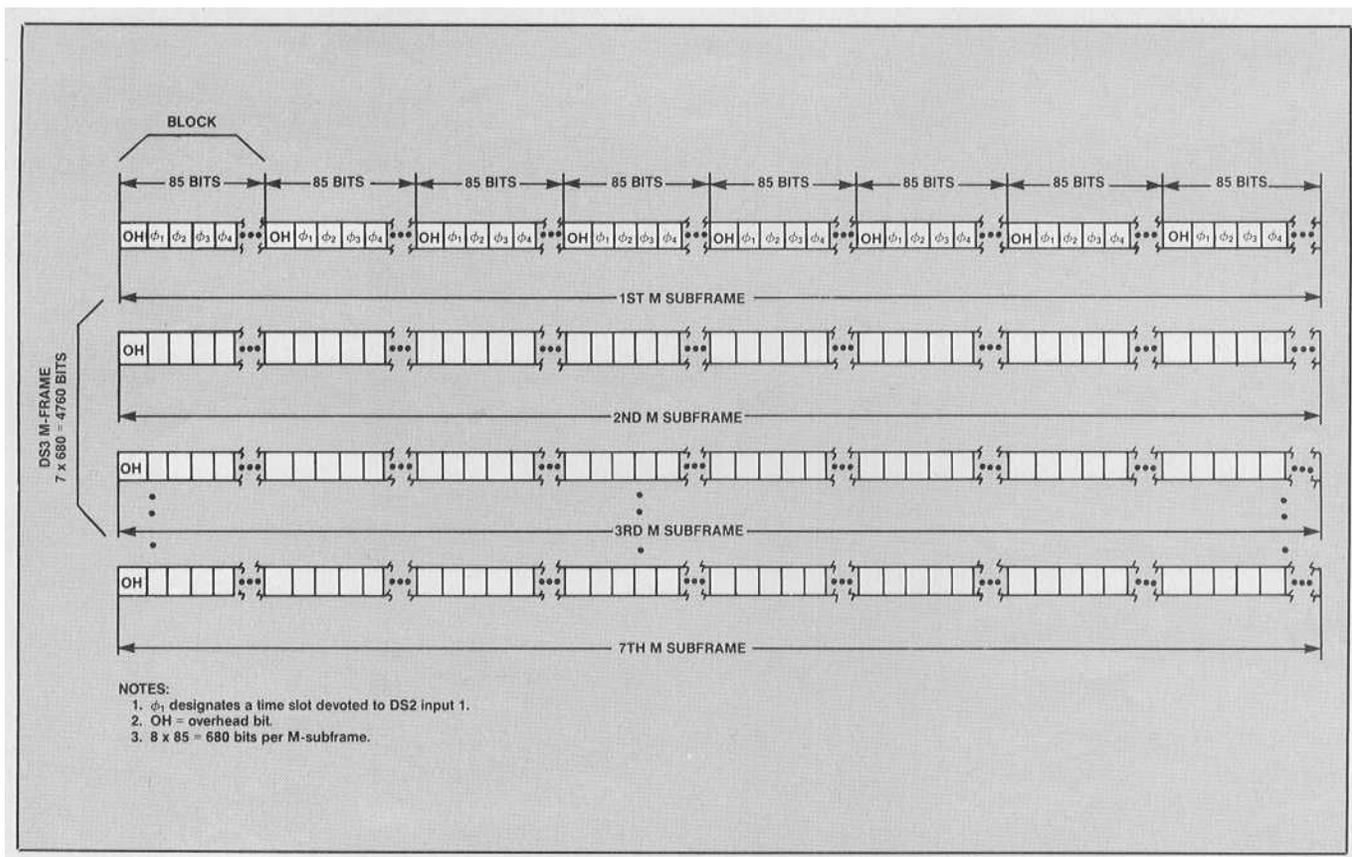


Fig. 4. DS3 Framing Format.

particular subframe. (C-bits will be discussed in greater detail in Part II.)

#### DS3 FRAMING FORMAT

The second step in forming a DS3 signal is to multiplex seven DS2 signals (each containing four DS1 signals) into a DS3 signal. The same method that is used to multiplex the four DS1 signals into a DS2 signal applies. Figure 4 shows the DS3 framing format, known as the standard M13 asynchronous format. M13 is the multiplex designation for multiplexing 28 DS1 signals into one DS3 signal. The DS3 frame (sometimes called a DS3 M-frame) is composed of seven subframes, designated one through seven. Each subframe consists of eight blocks and each block contains 85 bits. The first bit in each block is a DS3 overhead bit. Each DS3 frame contains 56 of these overhead bits (1 overhead bit per block x 8 blocks per subframe x 7 subframes per DS3 frame). The remaining 84 bits in a block are DS2 information bits. The total number of DS2 information bits in a DS3 frame is:

$$\begin{aligned} &84 \text{ DS2 bits/block} \times 8 \text{ blocks/subframe} \\ &\quad \times 7 \text{ subframes/DS3 frame} \\ &= 4704 \text{ DS2 information bits.} \end{aligned}$$

The seven subframes do not represent each of the separate DS2 signals. Instead, the DS3 frame is formed by bit-by-bit interleaving of the seven DS2 signals, as demonstrated in Figure 4. This interleaving process is the same as that used when the four DS1 signals are multiplexed together to form a DS2 signal. After every 84 DS2 information bits - 12 from each DS2 signal - a DS3 overhead bit is inserted. The total number of DS2 information bits transmitted in one second is:

$$\text{DS2 rate} \times 7 \text{ DS2 signals per DS3,}$$

which is:

$$6.312 \text{ Mbps} \times 7 \text{ DS2 signals} = 44.184 \text{ Mbps.}$$

The overall rate chosen for DS3 is 44.736 Mbps, providing extra bandwidth for DS3 bit stuffing and DS3 overhead bits.

#### DS3 Bit Stuffing

The seven DS2 signals may be asynchronous relative to each other (because they may not have been formed within a common multiplexer), and therefore may be operating at different rates. Bit stuffing is used to adjust the different incoming rates.

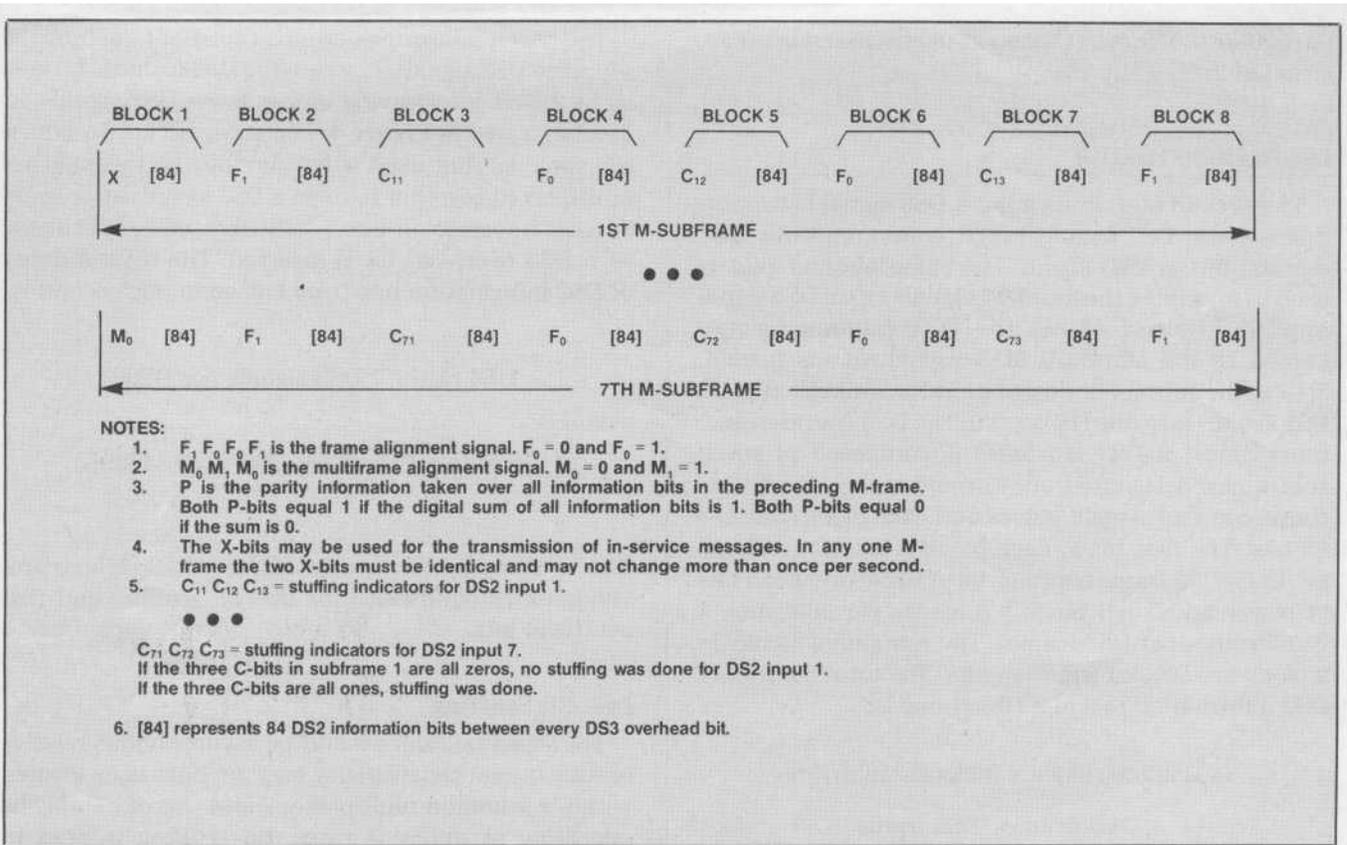


Fig. 5. DS3 Overhead Bits.

### DS3 Overhead Bits

The DS3 overhead bits provide alignment, error checking, in-band communications, and bit stuffing control information. The overhead bits are located in the first bit position of every block. Figure 5 shows the location of the various DS3 overhead bits.

#### F-bits

The F-bits (framing bits) form the frame-alignment signal. There are 28 F-bits per DS3 frame (four per subframe). The F-bits are located in the first bit position in blocks 2, 4, 6, and 8 of each subframe. The frame-alignment pattern, which is repeated every subframe, is "1001."

The rate of framing bit errors is a good in-service approximation of the logic bit error rate, because of the number and location of framing bits.

#### M-bits

The M-bits (multiframing bits) form the multiframe-alignment signal. There are three M-bits per DS3 frame. The M-bits are located in the first bit position in block 1 of subframes 5, 6, and 7. DS3 equipment uses the M-bit "010" pattern to locate the seven subframes.

#### C-bits

The C-bits are used to control bit stuffing. There are three C-bits per subframe, designated C<sub>i</sub>, (see Figure 5), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe.

## X-bits

The X-bits (message bits) may be used by a DS3 source for asynchronous in-service messages (i.e., the message is embedded in the data). There are two X-bits per DS3 frame. The X-bits are located in the first bit position in block 1 of subframe 1 and subframe 2. In any one DS3 frame the two X-bits must be identical, either both ones or both zeros. Also, the source may not change the state of the X-bits more than once every second.

## P-bits

The P-bits (parity bits) contain parity information. There are two P-bits per DS3 frame. The P-bits are located in the first bit position in block 1 of subframe 3 and subframe 4. DS3 sources compute parity over all 4704 DS3 information bits (4760 total bits - 56 overhead bits) following the first X-bit in a DS3 frame. The resulting parity information is inserted in the P-bit positions of the following frame. The state of the two P-bits within a single DS3 frame is always identical. The two P-bits are set to "1" if the previous DS3 frame contained an odd number of ones. Conversely, the two P-bits are set to "0" if the previous DS3 frame contained an even number of ones.

The parity bits provide a means of in-service error detection. If, on the receive-side, the number of ones for a given frame does not match the parity information in the following frame, one or more bit errors occurred during the transmission.

## CONCLUSIONS

To review, the DS3 signal is composed of 28 DS1 signals and is constructed using a two-step multiplexing process. First, the 28 DS1 signals are multiplexed into seven DS2 signals. Next, the seven DS2 signals are multiplexed into one DS3 signal. Each multiplexing step uses bit stuffing to handle the different input frequencies. Overhead bits provide alignment, error checking, in-band communications, and bit stuffing control information.

As DS3 continues to grow, so does the need for improved DS3 network maintenance. A new DS3 framing format, called C-bit parity, provides additional maintenance functionality. In the second half of this article, the C-bit parity framing format will be discussed.

*Gregory R. Werth is a product marketing manager for Telecommunications Techniques Corp. (TTC), where he is responsible for DS3 test products. Before joining TTC Mr. Werth worked for Hughes Network Systems. He holds a BSEE and an MSEE from the University of Michigan.*